REMARKS

This Amendment is responsive to the Office action mailed on March 18, 2002. A Petition for a 1-month extension of time is attached so that the due date for response is July 18, 2002.

In this Amendment, independent claims 1, 10, and 24 are amended to incorporate the limitations in claims 4, 11, and 25. Claim 9 is amended so that it is in independent form. Claims 4, 11, and 25 are canceled. Since amended claims 1, 9, 10, and 24 are the same as previously submitted claims 4, 9, 11, and 25, respectively, amended claims 1, 9, 10, and 24 do not raise new issues necessitating a new search or different consideration by the Examiner.

New claim 29 is added. Claims 1-3, 5-10, 12-24, and 26-29 are pending and subject to examination on the merits. No new matter is added.

35 USC § 102(b)

Claims 1-7, 9, 10, 12, 13, 17, 18, 19, and 24-28 are rejected as anticipated by U.S. Patent No. 5,892,271 ("Takeda"). Applicant traverses this rejection.

Takeda does not anticipate claims 1, 10, and 24 as originally filed. However, in order to expedite the prosecution of this application, these claims are amended to incorporate the limitations in claims 4, 11, and 25. Accordingly, independent claims 1, 10, and 24 are essentially the same as previously submitted dependent claims 4, 11, and 25. The anticipation rejection as to claim 10 should be obviated, since dependent claim 11 was not rejected as anticipated by Takeda.

As to claims 1 and 24, Takeda does not anticipate independent claims 1 and 24, or any claims that are dependent thereon. In the anticipation rejection, the Examiner cites FIG. 7 of Takeda as showing "a metal carrier member (8) [which] has a plurality of stamped bumps formed therein, i.e. the raised end portions which contact the solder bumps (3) on the semiconductor die. As can also be seen in FIG. 8 of Takeda, additional bumps (13) are formed on the opposite side of the carrier so as to electrically couple the die to a circuit substrate, as claimed."

Takeda does not teach a semiconductor die package, the carrier comprising: (a) a metal layer; and (b) a plurality of bumps formed in the metal layer, wherein the carrier is for electrically coupling the semiconductor die to a circuit substrate, and wherein the carrier further comprises a die attach region, and wherein the plurality of bumps are arranged around the die attached region as recited in independent claim 1. Referring to FIG. 7 of Takeda, the raised portions of the conductive leads 8 under the solder bumps 3 are under a semiconductor chip 1. Assuming *arguendo* that these raised portions are even "bumps," they are not "arranged around [a] die attach region." but are under a semiconductor chip and are therefore within the die attach region.

There is also no motivation to modify Takeda so that the raised portions of the conductive leads 8 and the solder bumps 3 are around a die attach region. If Takeda was modified to have the raised portions of the conductive leads 8 and the solder bumps 3 on the raised portions around the region on which the semiconductor die 1 is attached, the solder bumps 3 would not be in contact with the semiconductor die 1 and the semiconductor die 1 would have no input or output connections. Accordingly, there is no motivation to modify Takeda to arrive at the inventions defined by the claims.

Independent claim 24 recites a method including, *inter alia*, "(b) forming a plurality of bumps in the metal layer, wherein the formed bumps are capable of being electrically coupled to conductive regions of a circuit substrate, and wherein forming the plurality of bumps comprises stamping". Applicant has reviewed Takeda and cannot find the word "stamping" anywhere in it. Accordingly, Takeda does not teach or suggest the method recited in claim 24.

With respect to claims 9, 17, and 29 in particular, Takeda clearly fails to teach or suggest "conical" bumps. Assuming *arguendo* that the raised portions of the leads 8 shown in FIG. 7 of Takeda can even be characterized as "bumps", they are certainly not conical, but appear to be curved portions of strips of metal. A curve in a strip of metal is not a conical bump. Accordingly, claims 9, 17, and 29 (and any claims depending thereon) should clearly be patentable over the art of record as there is no teaching or

suggestion of a metal layer with conical metal bumps formed in the metal layer in any of the references of record.

35 USC § 103

Claims 8, 11, 14-16, and 20-23 are rejected as unpatentable over "Takeda, and further in view of applicant's admitted prior art as discussed in page 1 of the specification, as related to prior art FIG. 1, and Akram." This rejection is traversed.

The obviousness rejection is improper. The obviousness rejection is based on "applicant's admitted prior art." However, Applicant has not admitted that any embodiment described in the specification is prior art. Applicant has reviewed the Background of the Invention section of the present patent application and cannot find the words "prior art" anywhere in it. Accordingly, it is unclear how the Examiner can presume that the embodiment shown in FIG. 1, for example, is "prior art". Since no admission of prior art has been made, the obviousness rejection is improper and should be withdrawn for this reason alone.

Even assuming *arguendo* that it is even proper to use Applicant's Background of the Invention section of the present patent application to render Applicant's own claims obvious, there is also no motivation to make the combination proposed by the Examiner. The Examiner states that "the motivation for including such [vertical] MOSFETs to the Takeda semiconductor die would be the obvious fact that MOSFET devices are routinely included in semiconductor integrated circuits as described by Takeda." However, contrary to the Examiner's proposal, one would not have been motivated to modify Takeda's semiconductor chip 1 to include a vertical MOSFET. As explained at page 11, lines 10-14 of the present specification, a vertical MOSFET has a source at one side of a semiconductor die and a drain at the other side of the die so that current flows vertically through the semiconductor die. Thus, a die with a vertical MOSFET has an electrical input at one side of the die and an electrical output at the other side of the die. In FIG. 2 of the present application, for example, bumps 26 provide a connection to one side of the die 40 while solder balls 42 provide a connection to the other side of the die 40. No such

structure is shown in FIG. 7 of Takeda. In FIG. 7 of Takeda, the chip 1 has electrical connections on only one side, and one skilled in the art would not have been led to incorporate a vertical MOSFET into the chip 1 since there is no electrical connection on the side of the chip 1 that is opposite to the flexible substrate 4.

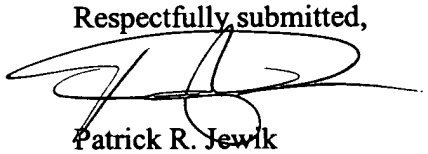
The Examiner also alleges that "Takeda does not specifically discuss the dimensions of the carrier bumps in his device, Akram shows a similar device using a bump mounted carrier plate to attach a semiconductor die, where the bumps have a thickness equal to or greater than the thickness of the semiconductor die." In response, it is believed that the "bumps" referred to by the Examiner are the bumps 50 in FIGS. 2-3 of Takeda. These bumps 50, however, are bumps that include a conductive material like solder (see col. 5, lines 15-28). They are not bumps that are formed in a metal layer. Accordingly, Akram fails to remedy the deficiencies of Takeda.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-273-7529.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 4, 11, and 25 are canceled.

1. (Amended) A carrier for a semiconductor die package, the carrier comprising:

(a) a metal layer; and

(b) a plurality of bumps formed in the metal layer,

wherein the carrier is for electrically coupling the semiconductor die to a circuit substrate, and wherein the carrier further comprises a die attach region, and wherein the plurality of bumps are arranged around the die attached region.

9. (Amended) [The carrier of claim 1] A carrier for a semiconductor die package, the carrier comprising:

(a) a metal layer; and

(b) a plurality of bumps formed in the metal layer,

wherein the carrier is for electrically coupling the semiconductor die to a circuit substrate, and wherein each bump has a conical shape.

10. (Amended) A semiconductor die package comprising:

(a) a carrier comprising a metal layer, a die attach region, and a plurality of bumps formed in the metal layer; and

(b) a semiconductor die electrically coupled to the die attach region of the carrier, and wherein the plurality of bumps are stamped bumps and are arranged around the die attach region, and wherein each of the bumps has a height that is greater than or equal to a thickness of the semiconductor die.

24. (Amended) A method for forming a carrier for a semiconductor die package, the method comprising:

(a) providing a metal layer; and

(b) forming a plurality of bumps in the metal layer, wherein the formed bumps are capable of being electrically coupled to conductive regions of a circuit substrate, and wherein forming the plurality of bumps comprises stamping.

29. (New) The method of claim 24 wherein the bumps each have a conical shape.